AMENDMENTS TO THE CLAIMS:

1.(currently amended): An interface device for establishing an interface between a CPU and an external unit, comprising:

a timer portion,

a mask portion, and

an interrupt controlling portion, wherein:

said timer portion asserts a mask signal when detecting that a wait signal outputted from said external unit is kept asserted for more than a predetermined period of time,

said mask portion masks said wait signal and outputs it to said CPU when said mask signal is asserted; and

said interrupt controlling portion issues an interrupt signal to said CPU when said mask signal is asserted.

2. (currently amended): An information processing system comprising a CPU and an interface device for establishing an interface between said CPU and an external unit, wherein:

when said interface device detects that a wait signal outputted from said external unit has been kept asserted for more than a predetermined period of time, said interface device masks the wait signal for outputting to said CPU and issues an interrupt signal to said CPU to prevent freezing of the information processing system caused by occupation of a bus of the information processing system when said wait signal has been kept asserted.

3. (previously presented): An information processing system according to Claim 2, wherein said interface device includes a timer portion, a mask portion and an interrupt controlling portion, wherein

said timer portion is activated when the wait signal outputted from said external unit is asserted, and then asserts a mask signal when said wait signal is kept asserted for more than a predetermined period of time;

said mask portion masks said wait signal for outputting to said CPU when said mask signal is asserted; and

said interrupt controlling portion issues an interrupt signal to said CPU when said mask signal is asserted.

4. (original): An information processing system according to Claim 3, wherein said CPU detects said interrupt signal thereby to recover said external unit.

5.(original): An information processing system according to Claim 2, wherein said CPU detects said interrupt signal thereby to recover said external unit.